Form PTO 1449 (Modified)	U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE	ATTY DOCKET NO.	SERIAL NO.
		241280US2S DIV	New Application
LIST OF REFERENCES CITED BY APPLICANT		APPLICANT	
		Tsutomu SATO et al.	
		FILING DATE	GROUP
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NN	AW	Robert HANNON, et al., "0.25^{m}m Merged Bulk DRAM and SOI Logic Using Patterned SOI", 2000 Symposium on VLSI, TECHNOLOGY DIGEST OF TECHNICAL PAPERS, (2 pages)
NN	AX	H.L. HO, et al., "A 0.13μm High-Performance SOI Logic Technology with Embedded DRAM for System-On-A-Chip Application", 2001 IEDM TECHNICAL DIGEST, (4 pages)
	AY	
	AZ	☐ Additional References sheet(s) attached

Examiner NHuu V Nyo — Date Considered 11-4-04

*Examiner: Initial if reference is considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.